

APPENDIX H

Figure 8 is a logic diagram illustrating a prior art quad signaling level transmit circuit. A fixed logic zero signal is coupled at node 801 to an input of a shift register comprising flip-flops 815, 817, 819, and 821. A load signal for performing a parallel data load of the shift register is provided to the shift register at node 803. A transmit clock signal is provided to a clock input of the shift register at node 805. Nodes 807, 809, 811, and 813 are coupled to parallel load data inputs of flip-flops 815, 817, 819, and 821, respectively. A serial data output of the shift register at the output of flip-flop 821 is coupled to an input of multiplexer 826 at node 823.